ISSN : 2347 - 2243

Indo - American Journal of Life Sciences and Biotechnology

www.iajlb.com
Email : editor@iajlb.com or iajlb.editor@gamil.com

Indo-American Journal of Life Sciences and Biotechnology

Vol.19, Issue.2, May 2022

Design and Analysis of Low Power, High Performance 2-4and4-16Mixed-Logic Line Decoders

P.Maheswari1,K.SuneelBabu2

Abstract:

Line decoders are being designed using a mixed-logic approach that incorporates transmission gate logic, dual-value logic using pass transistors, and static CMOS. The 2-4 decoders are given with two new topologies. 14-transistor and 15-transistor topologies attempting to minimize transistor count and power dissipation, respectively. A normal and an inverted decoder is used in each situation to create a total of four unique designs. Four novel decoders for the 4-16 range have been built, using mixed-logic 2-4 pre-decoders and a regular CMOS post-decoder. As opposed to their typical CMOS counterparts, all of the proposed decoders feature full swinging functionality and a significantly decreased transistor count. At the 32nm node, the suggested circuits offer significant improvements in power and latency over CMOS in almost all circumstances, according to a range of comparative computer simulations.

IndexTerms— transmission gate, line decoder, mixed logic, and pass transistor logic logic.

I.**INTRODUCTION**

Even if all electronic gadgets are in digital format, the concept of digital data manipulation has a positive impact on society. We are currently in the VLSI era because of the development of many digital IC technologies. There are both advantages and disadvantages to using these digital technology. When the Bipolar Junction Technology (BJT) was invented, it allowed the first IC, TTL, to be built (Transistor- Transistor Logic). In terms of packing density, TTL logic is superior, but in terms of turnoff time, it falls short. ECL (emitter coupled logic) is a novel technology that is faster than current logic but has a larger power dissipation. MOS technology, on the other hand, defeats BJT in the VLSI age. A lower power dissipation and higher packing density are provided by MOS in comparison to BJT. For static properties like lowest static power dissipation and the greatest Noise margin, CMOS technology beat MOS technology once again. It's just that the dynamic power dissipation and digital switchingnoise of CMOS ICs are a concern.

Differential amplifiers are the answer to this conundrum. We can bias and couple the amplifier stage together without the use of a bypass or coupling capacitor with these amplifiers, which are less sensitive

1PGStudent,Dept.ofECE(VLSI&ES),SSNEngineeringCollege,Ongole,AP,India.
2AssistantProfessor,Dept.ofECE,SSNEngineeringCollege,Ongole,AP,India.

to noise. SCL (source coupled logic), FSCL (folded source coupled logic), and MCML (source coupled logic) were all developed as a result of this (MOS current Mode Logic). Static CMOS logic has a number of advantages in constructing digital circuits, including low noise sensitivity, high performance, low power consumption, and more. However, when it comes to creating mixed-mode ICs, it has significant drawbacks. Multiple logic gates switch at the same time in a VLSI circuit, resulting in switching noise. Due to substrate coupling, the mixed-mode IC incorporates both analog and digital circuits on a single semiconductor die. As a result, mixed-mode ICs are slower and less precise. Diverse techniques, such as using separate analog and digital supply lines, a diffuse guard band, and bonding pads, are employed to decrease noise in mixed-mode ICs. It has been found to be the most effective approach of all the constant current source techniques for reducing digital switching noise, called source coupled logic (SCL).Modern technology faces a huge problem with power consumption reduction. Microprocessors, Digital Signal Processors (DSPs), and other high-performance digital systems require low power design. Complex semiconductors with high clock frequencies are theresult of a combination of chip density and operation speed. There is a pressing need for low-power VLSI circuit design due to the growing popularity of portable consumer electronics. items derived from the electronic industry When a binary integer value is fed into a decoder, the result is a certain pattern of output bits. Data de-multiplexing, memory address decoding, and seven-segment displays are just a few of the many uses for decoders. Codes are encoded into a series of signals via decoding, which is a relatively simple circuit. It's known as to begin our study of data conversion, we'll start with encoders and decoders because they are easier to construct than the huge coded data they transform. There are only a limited number of active instructions in the entire set of allin structions.

II.**Existing System**

As the name suggests, digital systems use binary codes to represent finite amounts of information. An n-bit binary code can have up to 2n unique bits. If the encoded information has vacant combinations, it is possible to decode binary information from n input lines to 2n different outputs, or less. Combinational circuits are used in decoders. n-to-m decoders generate the m = 2nminterms of n input variables, which are the circuits studied in this study.

Two to Four Lines of Text Decoder

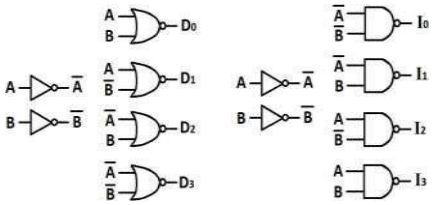
A and B are sent into a 2-4 line decoder, which outputs the four smallest terms D0-3. The table sums up its logic.I. Depending on the input combination, one of the four outputs is selected and set to 1, while the others are set to 0. Minterms I0-3 are complementary.generated by an inverting 2-4 decoder, and the selected output is set to 0, as indicated in Table II.TABLEITABLEII

TRUTH TABLE OF2-4DECODERTRUTH TABLE OF INV. 2-4DECODER

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

A	B	I_0	I_1	I_2	I_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

NAND and NOR gates are preferred over AND and OR in traditional CMOS design because they may be implemented with four



transistors instead of six. The 2-4 decoder can be built with the help of two inverters and four NOR gates if you have 20 transistors to spare (a). A 20-transistor invertingdecoder can be built using two inverters and four NAND gates, as shown in Fig. 1. (b).

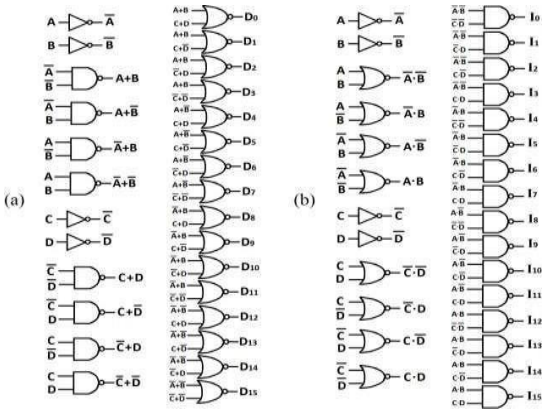
(a) (b)

Fig1. NAND and NOR decoders are implemented in CMOS logic-based 20-transistor 2-4 line decoders (b)

A. Decoder for 4-16 lines with 2-4 predecoders

A 4-16-line decoder and an inverting 4-16-line create MintermsD0-15 and I0-15, respectively. decoder, respectively, based on four input variables A, B, C, and D. 16 4-input NOR and NAND gates would be needed for the simplest implementation of these circuits. As an alternative, a predecoding technique can be used in which blocks of n address bits are predecoded into 1-of-2npredecoded lines that serve as inputs to the final stage decoder [1]. Using two 2-4 inverting decoders and sixteen 2-input NOR gates, a 4-16 decoder can be built using this manner.

Fig.2.104-transistor4-16linedecodersimplementedwith



CMOS logic and predecoding: (a) Non-inverting decoderimplemented with two 2-4 inverting predecoders and aNOR-based post-decoder, (b) Inverting decoder

III.A NAND-based post-decoder is used in place of two or more non-inverting predecoders.

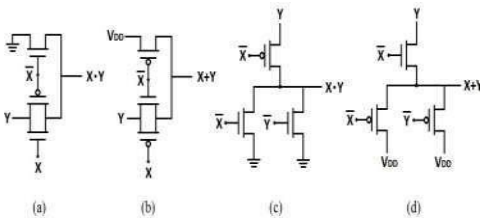
IV. Fig. 2(b) shows the implementation of a 2-4 decoder and 16 2-input NAND gates. 8 inverters and 24 4-input gates are needed for each of these designs in CMOS logic, generating 104 transistors altogether.

PROPOSEDDESIGN

When it comes to XOR-based logic, transmission gates are most commonly utilized in circuits like complete adders and multiplexers. Line decoders, for example, can benefit from their ability to implement AND/OR logic, as seen in [5]. Figures 3(a) and 3(b) demonstrate the 2-input TGL AND/OR gates. They're in full swing, but not all input combinations are being restored.

With regard to nMOS only pass-transistor circuits, like CPL [3], there are two primary circuit styles: those that employ nMOS and pMOS pass-transistor circuits, like DPL [4] and DVL [6]. DVL, a form that improves on DPL by retaining full swing functioning with a lower transistor count, is considered in this work[10]. The2-

Figures 3(c) and 3(d) illustrate inputDVLAND/ORgates. They are full-swinging but non-restoring, like TGL gates. The TGL/DVL gates require only three transistors instead of the four required by the4required in CMOS NAND/NOR gates. Decoders arehigh fan-



14 is the Fig. 3. The 3-transistor AND/OR gates considered in thiswork(a) TGL ANDgate, (b) TGL ORgate, (c) DVLANDgate, (d) DVLOR gate.

out circuits, wherefew inverters can be usedbymultiple gates, thus using the TGL/DVLgatescanresulttoreducedtransistor count.

An important common characteristic of these gatesis their asymmetric nature, ie the fact that they do nothave balanced input loads. As shown in Fig. 3, welabeledthe 2 gate inputs Xand Y. In TGL gates,inputXcontrolsthegateterminals ofall 3 transistors, while input Y propagates to the

transmission gate to the output node. This means that in DVL gates, two transistor gate terminals are controlled by an input, whereas one output transistor is controlled by an input. Control and propagation signals will be used interchangeably in this article.

This asymmetry feature allows a designer to execute signal arrangement, i.e. choosing which input is used as control and which as propagate signal in each gate. An inverter in the propagation line increases delay greatly, making it undesirable to use complimentary inputs as propagation signals. It is therefore more effective to use the inverted variable as the control signal when using the inhibition (A'B') or implication (A'+B' function). The AND (AB) or OR (A+B) function can be implemented in either way, and both work just as well. Finally, implementing either the NAND (A'+B') or NOR (A'B') function results in a propagation signal that is forced to be complementary.

a. The 2-4 Low-PowerTopology with 14 transistors

TGL or DVL gates would necessitate the use of a total of 16 transistors in a 2-4 line decoder design. Although it is feasible to delete one of the two inverters by applying proper signal organization and mixing both AND gate types into the same topology, the overall transistor count can be reduced to 14.

Suppose we want to remove the B inverter from the circuit since we only have two inputs, A and B. As the propagation signal, DVL gates are used to implement the Dominterm (A"B"). The TGL gate is utilized to implement the D1minterm (AB'), with B serving as the propagate signal. To implement the D2 minterm (A'B), A is used as the propagating signal in a DVL gate. It's finally accomplished with a TGL gate, where B serves as the propagation signal for D3minterm (AB). As a result of these design decisions, the complimentary B signal is never used.

A 14-transistor architecture can be achieved by removing the inverter from the circuit (9 nMOS, 5 pMOS).If you use OR gates instead, you can build a 2-4 inverting line decoder with just 14 transistors (five of which are MOS and nine of which are pMOS) by following a similar technique (using A as propagate signal). It is now possible to remove the B inverter from the circuit.

As a result of eliminating the inverter's role in the circuits, the overall power consumption of the circuits is reduced. The writers believe that bare minimum.

numberoftransistorsrequiredtorealizeafull-swinging2-4 line decoderwithstatic(non-

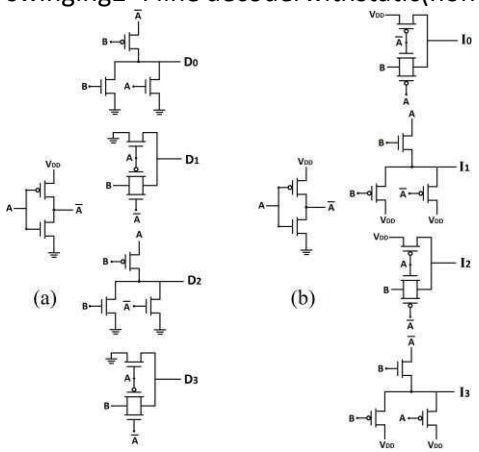


Figure 4: New 14-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LPI. timed) logic (Fig. 4a, 2-4LPI). Both of the new topologies, referred to as "2-4LP" and "2-4LPI," are based on the 'low power' and 'inverting' suffixes of the preceding names. As depicted in Figure 4(a) and (b), their schematics are depicted, respectively.

a. The 2-4 High-PerformanceTopology of 15 transistors

The use of complimentary A as the propagate signal in the case of D0 and I3 in the low-power

topologies described above has the disadvantage of a worst-case delay. Due to the lack of a requirement for complementary signals, it is possible to use ordinary CMOS gates to build D0 and I3. With the addition of one transistor to each topology, D0 can be implemented as a CMOS NAND gate and I3 as a CMOS NOR gate. Delay improvement and power consumption are both improved by this innovation, which incorporates three different types of logic into one circuit. Their names are "2-4HP" (nMOS, 6 pMOS), which stands for "high performance" (HP), and "2-4HPI" (nMOS, 9 pMOS), which stands for "inverting" (I). According to the "HP" suffix, these decoders have low power consumption and short delay times that result in an overall good performance. There are more transistors in the 2-4HPI and 2-4HP designs, which may be seen in the schematics in Figures 5(a) and 5(b), respectively.

LineDecoder Integration in the Range of 4-16

As contrast to static CMOS, circuits based on pass transistor logic can achieve logic functions with a less number of transistors and higher performance. When multiple non-restorative circuits are chained together, their performance begins to deteriorate much more quickly. Alternating restoring and non-restoring levels of logic, or "mixed topology",

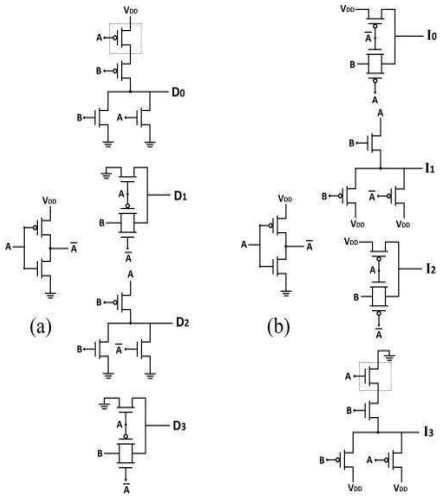


Fig.5.New 2-4 line decoders with 15 transistors: 2-4HP and 2-4HPI.

achieve the best possible outcomes by fusing their respective beneficial traits.

The four new 2-4 decoders were used as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs in accordance with the theory described in section II. In this combination, two 2- 4LPI predecoders are combined with two 2-4HPI predecoders, and the result is four new topologies: 4-16LP (Fig. 6(a)), which combines two 2-4LPI predecoders with a NAND post-decoder, 4- 16HPI (Fig. 6(b)), which incorporates two 2-4HP predecoders with a NAND post decoding unit and, finally, 4-16HPI (Fig. 6(d)), which incorporates two 2-4HP predecoders with a NAND post decoding unit..

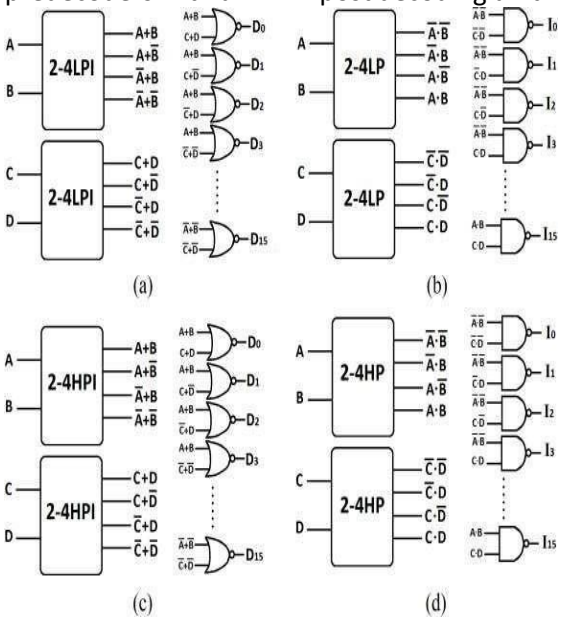


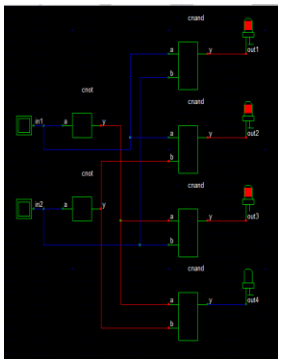
Fig.6.New4-16linedecoders:(a) 4-16LP,(b)4-16LPI, (c)4-
16HP,(d)4-16HPI.

The 'LP' topologies have a total of 92 transistors,while the'HP' ones have 94, as opposed to the 104transistorsrequiredbythepureCMOSimplementation.

SIMULATION RESULT AND COMPARISIONWith the 65nm CMOS process, Microwind built the suggested low-power, high-performance 2-4 and 4-16 line decoder circuits using PMOS transistors that are three times the size of

NMOS transistors. DSCH and microwind were used with a 1V power source for the simulations.

Using the DSCH 3.5 tool, the following simulation results and digital schematics demonstrate the capabilities of the full swing



GDI approach.

Fig7.SchematicofInvertingdecoderimplemented with2-4CMOSnon-invertingpredecodersandaNAND-basedpost-decoder

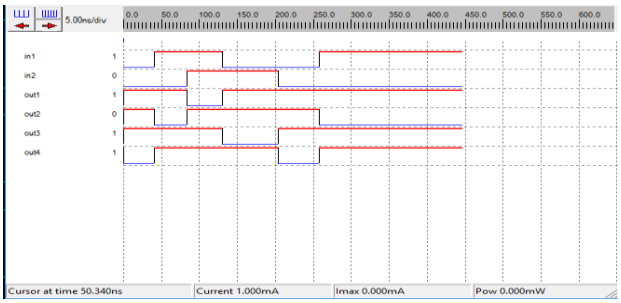


Fig 8. Simulation ofinverting decoders implemented with 2-4CMOSNAND

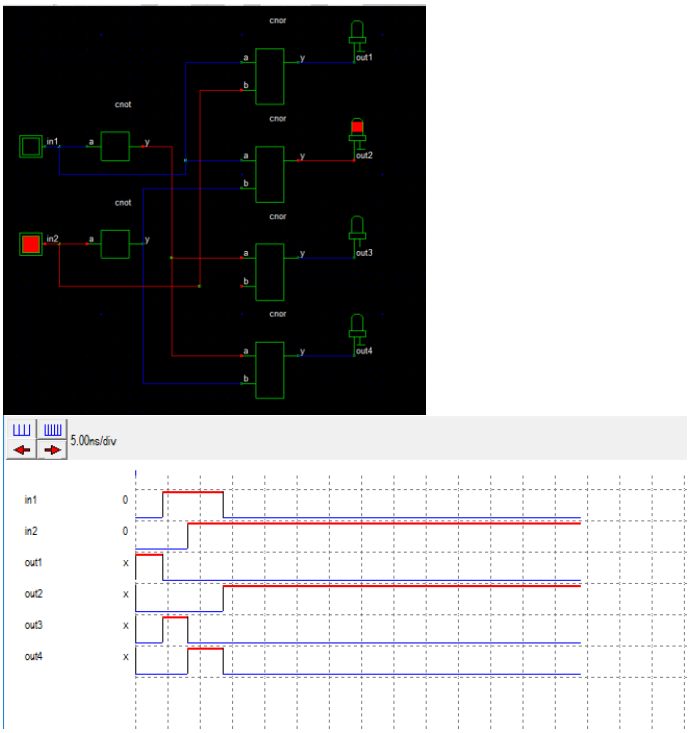


Fig10.Simulationofnon-invertingdecodersimplementedwith2-4 CMOSNOR

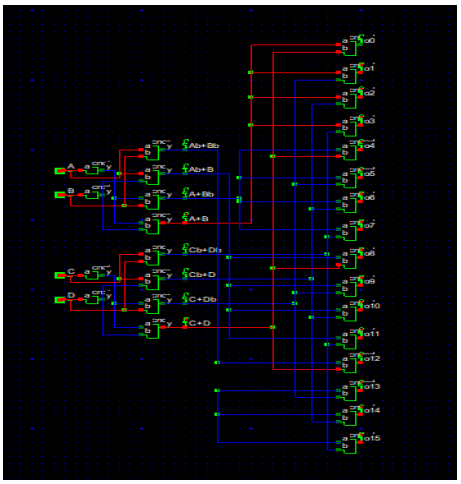


Fig32.Waveformof proposed 4-16 HPI decoder

All circuits are simulated at operating frequencies(5GHz)and supply/input voltages(1 V).

Design	Area(μm^2)	No" oftransistors	Power(µW)

4-16 CMOS NAND	1301.4	104	36.284
4-16 CMOS NOR	1350.6	104	38.533
4-16LP	1141.6	92	25.988
4-16LPI	1145.7	92	25.246
4-16HP	1190.2	94	24.033
4-16 HPI	1190.2	94	26.848

V. CONCLUSIONS

An efficient mixed-logic architecture for decoder circuits, incorporating TGL, DVL, and static CMOS, was introduced in this study. We designed four new 2-4 line decoder topologies based on this methodology: 2-4LP, 2-4LPI, 2-4HP, and 2- 4HPI, which have lower transistor counts (and thus a smaller layout area) and better power-delay performance than typical CMOS decoders.

It was also shown that there are now four new 4-16 line decoder topologies that can be created using the mixed-logic 2-4 decoders as predecoders and the static CMOS logic decoders as postdecoders. This type of design combines the advantages of pass transistor logic with static CMOS's ability to recover from failures.

At 65 nm, a number of comparative spice simulations were carried out, with the results showing that the proposed designs have a clear advantage..

For low power CMOS, V. G. Oklobdzija and B. Duchene developed "pass-transistor dual value logic." It's best to use the 2-4LP and 4-16LPI topologies if you're looking to reduce the size and power consumption of your system. It was found that the 2-4LPI, 2- 4HP, and 2-4HPI, as well as their four 16-topologies (four 16LP, four 16HPI, and four 16HP) were all viable designs that may serve as building blocks for more complex decoders and multiplexers with a wide range of performance requirements.

In addition, the reduced transistor count and low power features shown here can help both bulk CMOS and SOI design..... La out level implementation is required to make the circuits appropriate for inclusion in standard cell libraries and RTL design.

R FERENCES

[1]the 4th edition of "CMOS VLSI Design, a Circuits and Systems Perspective," published by Addison-Wesley in 2011, is a good place to start.

[2]"Low-Power Logic Styles: CMOS vs. Pass-Transistor Logic," IEEE Journal of Solid State Circuits, vol. 32, no. 7, pp.1079 - 1090, 1997.

[3]K. Yano et al., "A 3.8-ns CMOS 16x16-b multiplier employing complementary pass-transistor logic," IEEE J. Solid-State Circuits, vol. 25, pages 388-393, 1990.

[4] IEEE 1993 International Solid-State Circuits Conference Proc., pp.90-91, M. Suzuki et al., "A 1.5ns 32b CMOS ALU in double pass transistor logic."

[5] X. Wu, "The theory of transmission switches and its application to the design of CMOS digital circuits," International Journal of Circuit Theory and Application, vol. 20, no. 4, pp.349-356,1992.

[6] 34 1995

[7] Decreased energy usage in address decoders by selective precharge techniques, Microelectronics Journal, vol. 40, no. 11, pp. 1590-1600,2009, by M. A. Turi and J.G. Delgado-Frias [7].

[8] Optimizing a row decoder for a 256-by-256 6T SRAM using VLSI-SATA (VLSI Systems, Architecture, Technology, and Applications), VLSI-SATA, pp. 1-4 (VLSI-SATA 2015), Bhatnagar, Chandani, and Pandey (8). IEEE,2015.

[9]"Novel design technique of address Decoder for SRAM" was published by A. K Mishra, D. P. Acharya, and P. K. Patra in 2014.

[10]Advanced Communication Control and Computing Technologies (ICACCCT), IEEE, 2014, pp. 1032-1035.

[11](10) D. Marovi, B. Ni oli, and V. O lobdia, "A generic method in the fabrication of pass-transistor circuits," Microelectronics Journal, vol 31, pp 991-998,2000.

[12] Consult the following url for more information:
[13] IEE J. Solid State Circuits, 47(1):47-60, Jan. 2012. [11] N. Lotze, "A 62mV 0.13m 0.13m CMOS Standard-Cell-Based Design Technique using Schmitt-Trigger logic,"