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# Novel architecture of multiplier for Accuracy-scalable approximate computing

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**Abstract**—Many error-tolerant applications rely on multiplication as a fundamental function. Approximate multiplication is regarded as an efficient method for balancing performance and accuracy against energy consumption. As a result, this research presents a low-power and compact multiplier for accurate, scalable approximate computation. A carry-maskable adder and an approximate tree compressor (ATC) make up the proposed approximate multiplier (CMA). By adopting a simple circuit topology and a simple carry-masking technique, ATC compresses partial products while the CMA provides precision scaling. This approximate multiplier reduces both power consumption and circuit area when compared to the Wallace tree multiplier, according to the experimental designs.

**Keywords—**scalability, accuracy scalability, and approximation computation.

## INTRODUCTION

Applications like the ones described above all rely on multiplication as a fundamental process. In this case, a reduction in the cost of multiplication is beneficial. A rough multiplier is the subject of this study. Many approximate multipliers have been proposed[1,2, 3, 4, 5], but most of the preceding works lack precision scalability[2,3]. This limits the range of possible applications. For the following two reasons, dynamic configurability is essential.

Power efficiency is a need for many modern applications. Among other things, these applications are battery-powered and/or incorporated in the devices. Internet of Things (IoT) gadgets are a good example of this. Image processing, sensing, recognition, and machine learning are examples of applications that are inherently error tolerant. In cases where exact findings aren't necessary, results that are almost as accurate will do. To fulfill the goal for low power usage, approximation computing [1] is a viable technology. Accuracy can be exchanged for power in this manner.

To begin, the accuracy requirements of various apps vary, just as the functionality of various programs inside an application varies.

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If the accuracy of multiplication is fixed, power will be squandered when high accuracy isn't needed. The second consideration is relevant to iterative applications.approaches, the level of precision required changes over time[6, 7].

However, while some multipliers can be configured either statically [4] or dynamically [5], modern mobile devices such as IoT devices require smaller and lower-power multipliers even if precision is reduced.

This study examines the accuracy of a low-power, small-area multiplier.

What follows is a breakdown of the rest of the document: Next, we'll take a look at some of the earlier work. The proposed multiplier is then described. Finally, the conclusions are reached following the presentation of the experimental assessment data. scalableapproximatecomputing.

## I. LILERATUREWORK

An approximation of 4-2 compressors is used in Yang et almultiplier .'s [2]. In this paper, we refer to this multiplier as YHL15. YHL15 had a high level of accuracy because the study's goal was to meet the requirement of a low mistake rate. This research aims to demonstrate a low-power and small-area multiplier for use in applications with strict power and device volume requirements.

The ATC suggested by Yang et al. [3] was utilized to create the ATCM, an approximation of a multiplier. When using ATCM's four-compressor design, both power and accuracy are perfectly balanced. Power and latency are both reduced by this multiplier, but accuracy is sacrificed. For both power and area reduction, the multiplier described in this research uses the ATC's multiplier principle.

BothYHL15andATCMlackaccuracyscalability.

These two multipliers, however, can be scaled up or down.

An approximate adder and an error reduction circuit are used in Liu et almultiplier .'s [4] to reduce partial product and provide an error recovery vector. In this paper, we refer to this multiplier as LHL14.

It is possible to change the accuracy of LHL14's recovery vector by adjusting its bit width. On the other hand, the multiplier proposed in this article has a far higher degree of precision.

You can customize this paper as needed.

The CMA was proposed by Yang et al. [5] and was utilized to achieve the accuracy scalability in their multiplier by using the CMA. In this paper, we refer to this multiplier as YUS18. YUS18's dynamic configuration differs from LHL14's static configuration. Comparable to LHL14, it accomplishes a power accuracy trade-off. Although this article uses the concept of CMA for scalability purposes, the bit positions where CMA is applied have been carefully calibrated.

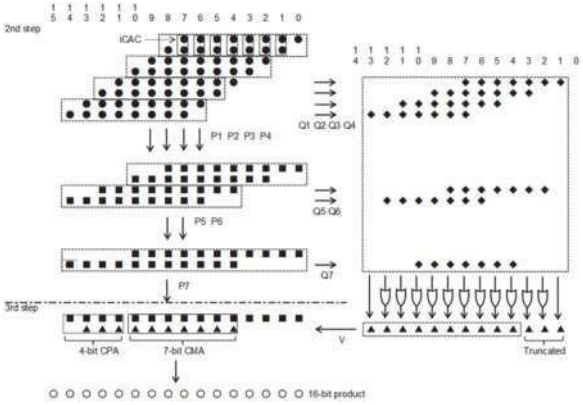



**Fig.1.Multiplicationflow.**

## II. EXISTINGMULTIPLIERS

A lower-power and smaller-area multiplier was created by modifying prior studies[3,5]. Using an approximation treecompressor (ATC)[3] to reduce the power and area of the multiplier at the cost of accuracy was frequently employed. Additionally, a CMA[5] was carefully adjusted to avoid major accuracy losses. In spite of the small size of this investigation, significant power savings were achieved. According to the most exact design, the proposed multiplier's power consumption was lowered by 68% and 41%, respectively, when compared to the Wallace tree and previously investigated multiplier[5]. To make matters worse, the suggested multiplier's surface area is 61.9% and 31.4% smaller than that of the other two multipliers combined

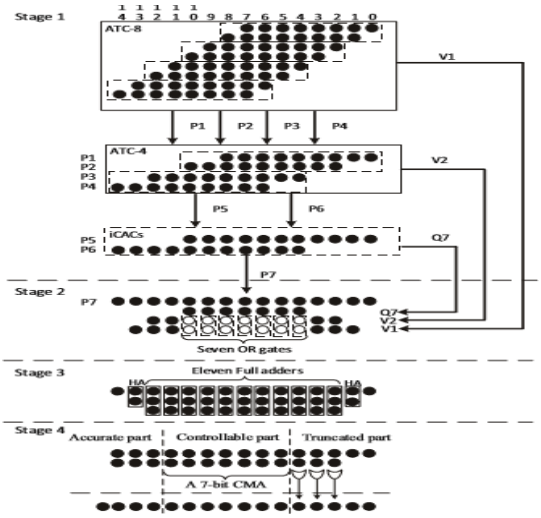



**Fig2.existingapproximatemultiplierdesign**[5]

## III. THE PROPOSED APPROXIMATEMULTIPLIER

Compressor-based multiplication is broken down into three parts. After generating the partial products, the partial products are reduced, and the total of reduced partial products is formed via a carrypropagationadder process (CPA).

The second and third steps of the proposed multiplier deal with approximation and configuration. Figure 1 depicts these procedures, which are further explained in the next sections.

A. ATCIt is shown in Figure 1 that a suggested 8-bit approximation multiplier contains 88 partial products.First, a 1-bit multiplicand is multiplied by a 1-bit multiplier on the same bitposition, and a 1-bit partial product is generated.The ATC[3] is used in the second phase to minimize the number of partial products by compressing the height of the partial product array.

[3] ATCs are made up of unfinished adder cells. iCACisshowninFig.2.

There is a half-adder in which the sums and the car ry co of two inputs, A and B, are expressed as a + b, where the sums and the car-ry co are expressed as c,s

Concatenation and addition are represented by the symbols,, and the plus sign (+).

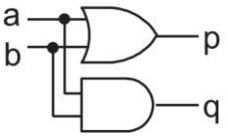
A+bisevidentfromthetruthtablewherepandqaret heoutputsofiCAC.

As a result, c,s = p + q and the iCAC can produce an exact sum.

**Consideran**

n-bitadditionofS=A+BwhereS={si|i=n—1,…0}, A={ai|i=n—1,…,0}andB={bi|i=n—1,…,0}.

Thecarry-outfromthemostsignificantbitisignored.Thus, n iCACsgeneratePandQfromAandB,whereP={pi|i=n— 1,…,0} andQ={qi|i=n—1,…,0}.Thetruthtableexplainsthatthe“1”sarecollected from AandBintoPandthatPisalwaysgreaterthanS.Hence,itcanbeseenthatPisanapproximatesumofAandB.Ontheotherhand,QworksasanerrorrecoveryvectortogeneratethepreciseſromP,becauseitisobviousthat S=P+Q.



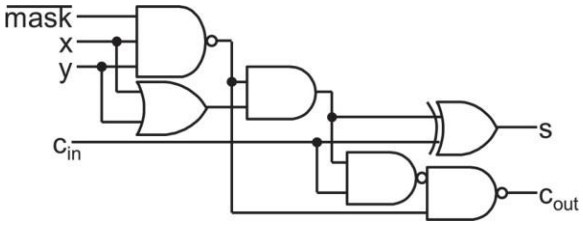

| a | b | q | p |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Fig.3.iCAC [3].

Fig. 1 depicts an example of this. A black circle denotes a partially completed object. The second stage includes three compression rounds. Seven iCACs operate eight x eight partial products in four groups of two rows each, resulting in four P and Q pairs. Individuals with the initials of their last names are recognized as such (P4, Q4). p and q are depicted as squares and diamonds in the picture. (P1, P2) to (P6, Q6), iCACs are utilized to operate every other row in the second round to construct P and Q pairs (P5, Q5) and (P6, Q6) respectively (P3, P4). P5 and P6 combine in the third round to generate P7 and Q7. Our latest acquisition is an estimate of an intermediate product designated P7. There are a total of seven recovery vectors to consider (Q1 through 7).

V is a single vector that combines all of the individual vectors seen in Fig.

Assume 1 is V.
When P7 and V are added together in the third phase, the precision of the approximation multiplier is calculated. In other words, the




accuracy depends on the condensing method used for the recovery vectors. For example, combining the vectors will give you an accurate result. Remember that the purpose of this research is to develop a low-power and small-area approximation multiplier. Condensing and generating the accuracy compensation vector from the error recovery vectors should be done with the simplest circuit possible. The OR gate is chosen as the circuit because it prevents a lot of mistake accumulation. expected. According to the truth table in Figure 3, "0" favors Q whereas "1" favors P. Thus,Qn(n=1,
A sparse vector like...,6 can be ORed together without causing any significant errors. At the most
significant bits are
omittedfromV because they aren't critical to the accuracy of the calculation.
A. CMA
CMA [5] configures the output product's precision in the third step.
Figure4 depicts a single bitCMA.
When m a s k = 1, the traditional full ladder is used.
Other than that, itscarryoutis hidden in order to prevent it from spreading, and its sum operates as follows: s=aORb.
The presumption is that CIN is also masked and equivalent to a 0
Because the most significant bits are so crucial to accuracy, the traditional CPA is used to sum them all together.

A 4-bit CPA is used in this design. The CMA is used to configure precision in the remaining bit locations. This is the case in his
The design, a7-bitCMA, was chosen.
The carry propagation is controlled by varying the width of the mask, and as a result, the
In this case, if the mask width is 4 bits, that is, ¯m¯¯a¯¯s¯k¯={1,1,1,0,0,0,0},
theupper3bitsoftheCMAwor
This is the exact CPA. An approximate product is then formed at this point.
The output is shown in Fig. 1 as white circles.

**Fig.4.CMA [5].**

## IV. SIMULATIONRESULTS

The proposed XILINX-ISE14 design is shown in the following RTL block diagram. There are two inputs [7:0] and one output [15:0] in the block diagram of the proposed

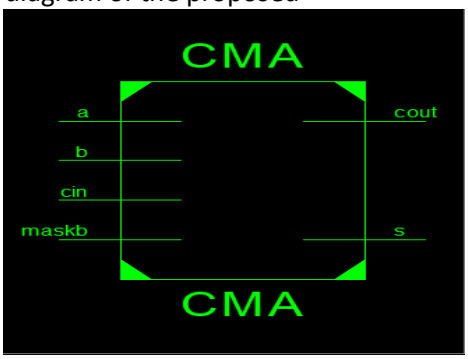



Fig5.1RTLblockofproposedCMA

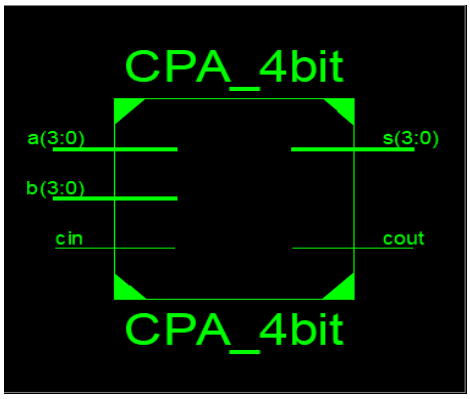



Fig5.2 RTLblockofproposed CPA
BelowfigureshowstheRTLblockdiagramofpropos edmultiplier

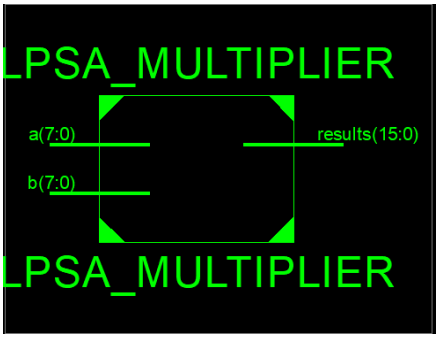
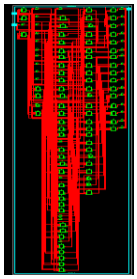



Fig5.3 RTLblockofproposed multiplier

Fig5.Using Xilinx ise 14, the proposed multiplier's internal RTL schematic is shown in Figure 4. Which is nothing more than the internal connections between the various blocks.



5.4RTLschematicofproposedmultiplier

The device usage summary is provided above, which provides the information about the number of devices used from the total number of devices accessible, as well as the percentage of those devices used. As a result of the synthesis process, the utilization of the device in the employed device and packaging is displayed below.

| CMA Project Status | | | |
|---|---|---|---|
| **Project File:** | multipler.xise | **Parser Errors:** | No Errors |
| **Module Name:** | CMA | **Implementation State:** | Synthesized |
| **Target Device:** | xc3s500e-5fg320 | **• Errors:** | |
| **Product Version:** | ISE 14.4 | **• Warnings:** | |
| **Design Goal:** | Balanced | **• Routing Results:** | |
| **Design Strategy:** | Xilinx Default (unlocked) | **• Timing Constraints:** | |
| **Environment:** | System Settings | **• Final Timing Score:** | |

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| Number of Slices | 1 | 4656 | 0% |
| Number of 4 input LUTs | 2 | 9312 | 0% |
| Number of bonded IOBs | 6 | 232 | 2% |

| Detailed Reports | | | | | |
|---|---|---|---|---|---|
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** |
| Synthesis Report | Current | Mon Nov 5 16:29:34 2018 | | | |
| Translation Report | | | | | |

Fig5.5 synthesisreportofproposedCMA

| CPA_4bit Project Status | | | |
|---|---|---|---|
| **Project File:** | multipler.xise | **Parser Errors:** | No Errors |
| **Module Name:** | CPA_4bit | **Implementation State:** | Synthesized |
| **Target Device:** | xc3s500e-5fg320 | **• Errors:** | |
| **Product Version:** | ISE 14.4 | **• Warnings:** | |
| **Design Goal:** | Balanced | **• Routing Results:** | |
| **Design Strategy:** | Xilinx Default (unlocked) | **• Timing Constraints:** | |
| **Environment:** | System Settings | **• Final Timing Score:** | |

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| Number of Slices | 4 | 4656 | 0% |
| Number of 4 input LUTs | 8 | 9312 | 0% |
| Number of bonded IOBs | 14 | 232 | 6% |

| Detailed Reports | | | | | |
|---|---|---|---|---|---|
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** |
| Synthesis Report | Current | Mon Nov 5 16:31:55 2018 | | | |

## V. CONCLUSION AND FUTURE SCOPEThe

Wallace tree multiplier and the previously proposed accuracy-scalable multiplier both use a lot of power, and this study suggests an approximation multiplier that may be adjusted for accuracy. The ratio of reduction depends on the accuracy desired. A last disadvantage of the suggested multiplier is that it occupies a lesser physical space than the existing multipliers. ATC and CMA ideas, which were carefully modified, were borrowed to achieve the lower power and smaller size. The simple circuit of the fundamental OR gates is used to construct the compensation vector at the cost of precision. Applications that emphasize power and area over accuracy and suffer from fluctuations under operating conditions, such as IoT devices, may benefit from this precision-configurable approximate multiplier.

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