ISSN : 2347 - 2243

Indo - American Journal of Life Sciences and Biotechnology

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Email : editor@iajlb.com or iajlb.editor@gamil.com

Indo-American Journal of Life Sciences and Biotechnology

Vol.19, Issue.2, June 2022

Novel Architecture of 4-bit Arithmetic Logic Unit (ALU) Using FullSwing GD I technique

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.**Abstract**—This study offers a design of a 4-bit arithmetic logic unit (ALU) by taking vantage of the concept of gate diffusion input (GDI) technique. ALU is the most significant and fundamental component of central processing unit as well as of numbers of embedded system and microprocessors. In this, ALU consists of 4x1 multiplexer, 2x1 multiplexer and low power full adder designed to implements logic operations. Full swing GDI cells are employed in the design of multiplexers and full adder which are then associated to realize ALU. The simulation is carried out DSCH3.5 and Microwind3.5 simulator utilizing 65nm technologies and compared with earlier designs realized with Pass transistor logic and CMOS logic.

Keywords—Assembled Arithmetic Logic (ALU), Full-Swing GDI, and Gate Diffusion Input.

I.**INTRODUCTION**

Any digital system would be incomplete without one. A microprocessor's ALU is one of its most important components. In a nutshell, the CPU is the brain of any system, and the ALU is the brain of the CPU. So it's a computer's brain in a brain. Fast dynamic logic circuits and precisely tuned architectures make up these devices. There is a large amount of CPU power consumption in any processor. Moreover, the ALU contributes to one of the highest power density areas on the processor, as it is clocked at the highest speed and is constantly busy, resulting in high temperatures and dramatic temperature gradients in the execution core. ALU designs that can meet the high performance requirements while also minimizing peak and average power consumption are greatly motivated by this.

Digital signal processing, microprocessors, image processing, and so on all require arithmetic operations in order to function.

Arithmetic operations that don't include addition aren't really arithmetic operations at all. A low-power high-performance adder cell is the most important consideration in the design of any arithmetic logic unit.In the design of a full adder cell, different topologies and Methodologies have been proposed. In the design of ALU and its sub-blocks, such as Multiplexer and Full Adder, this study makes use of the GDI method concept.

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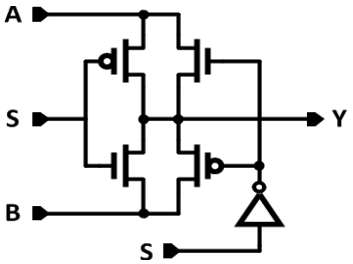
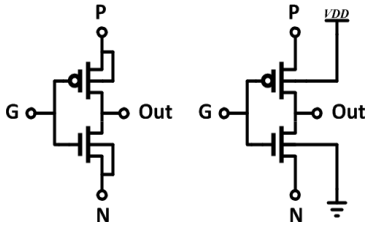
It is shown in this research that the 4-bit ALU may dissipate less power and use fewer transistors than prior designs because it makes use of the Full- Swing GDI approach to implement the low power adder cell.The following is how the paper is laid out: Section II provides an overview of the GDI methodology and discusses its advantages and drawbacks. Arithmetic logic units are explained in Section III, and simulation results and comparisons are presented in Section IV. Section V wraps up the entire piece.

GATEDIFUSSIONINPUTTECHNIQUEGDI

The novel Gate Diffusion Input Technique reduces power loss and propagation time while occupying a smaller footprint. GDI cells have



been used to create multiplexers and a full adder circuit in our ALU design. The ALU is implemented using a complete adder, while the input and output parts use 4x1 and 2x1



multiplexers. Researchers T. Esther Rani, M. Asha Rani, and Dr. RameshwarRao created an arithmetic and logic unit with an area optimized for minimal power consumption.

GDI and logic gates, as well as pass transistor logic, are used to implementFirst presented by ArkadiyMorgenshtein, IdanShwartz, and Alexander Fish [1], this technology permits the development of numerous sophisticated logic functions using only two transistors, as shown in Table I. In the beginning, the GDI relied on a simple cell, as depicted in Fig.1(a).

Fig. 1. GDI cell; (a) originally proposed, (b) standard CMOScompatible

TABLEI.DIFFERENTLOGICFUNCTIONSREALIZATIONUSINGGDICELL.

Two-by-one multiplexer is a digital switch that selects the output from a number of inputs based on a choose signal [4].

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Fig.2.Full-SwingGDI2x1Multiplexer

B.4x1Multiplexer

Fig. 3 shows a 4x1 multiplexer constructed using only 16 transistors, as detailed in the previous section on the 2x1 multiplexer.

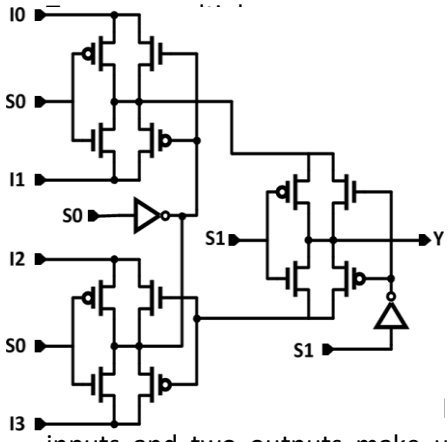
Sr. No.	Input			Output	Function
	P	G	N		
1	B	A	0	$A.\overline{B}$	F1
2	1	A	B	$A+\overline{B}$	F2
3	B	A	1	A + B	OR
4	0	A	B	A.B	AND
5	B	A	C	$A.\overline{B}+A.C$	MUX
6	1	A	0	$A\ \overline{\ }$	NOT

In [3] Full-Swing GDI cells, a transistor for swing restoration is employed to increase the output swing of F1 and F2 gates as an alternative to this technique's swing restoration buffers (universal gates used to realize any logical expression) For full swing operation, additional transistors are required but the area of the circuits is reduced, power is increased, and

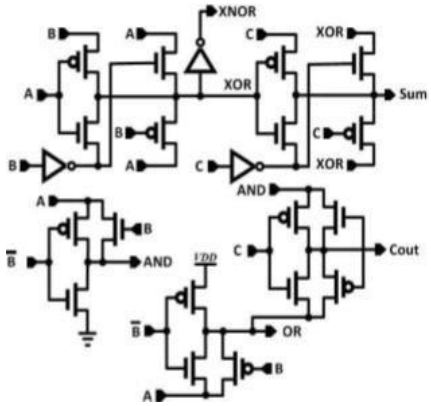
delay is reduced by utilizing fewer transistors than in CMOS implementations.

II.**ARITHMETICLOGICUNIT**

The following ALU design circuits are implemented using the Full-Swing GDI approach in this paper:



to make a full circuit. Three inputs and two outputs make up the system. Full-swing AND, OR, and XOR gates were employed to implement the adder cell in this design. Among three designs, this one was chosen because of its low power consumption,



the shortest delay of the three, and the ability to perform logic operations with minor alterations.

[5]aswell,thesemodificationswillsavelargeareaof theALU design.

Fig.4.Full-SwingGDIbasedFullAddercell

D.DesignofArithmeticLogicUnit

Arithmetic and logical operations are performed by the ALU in the CPU. The ALU is a combinational logic circuit, which means that the output varies as the input response changes. When it comes to microprocessors, the ALU comes in handy for a variety of logical and arithmetic functions. It is now possible to incorporate millions of transistors on a single chip because to the development of very large-scale integration (VLSI) technology. Due to its low power consumption and suitable mix component for analog and digital design, complementary metal oxide semiconductor (CMOS) has been the foundation of mixed signal. It can execute addition, subtraction, increment, and decrement math operations, as well as logic ones like AND, OR, XOR, and XNOR. With this new architecture, each stage of the 4-Bit ALU can be implemented using the previously stated circuits:

Two 2x1 multiplexers, two 4x1 multiplexers, and one full adder cell make up a 1-bit ALU stage, and this architecture necessitates 48 transistors, as shown in Fig. 5. The selection lines S0, S1, and S2 code can be used to perform any required operation, and Table II presents the truth table for the proposed ALU.

TABLE II. TRUTH TABLE OF THE PROPOSED 4-BIT ALU.

S2	S1	S0	Operations
0	0	0	DECREMENT
0	0	1	ADDITION
0	1	0	SUBSTRACTION
0	1	1	INCREMENT
1	0	0	AND
1	0	1	XOR
1	1	0	XNOR
1	1	1	OR

Based on the values of the S0 and S1 selection lines, a 4x1 multiplexer picks the B input on the S1 selection line. It's up to S2 to decide which of the arithmetic or logic operations to use for the Decrement, Addition, Subtraction, and Increment operations

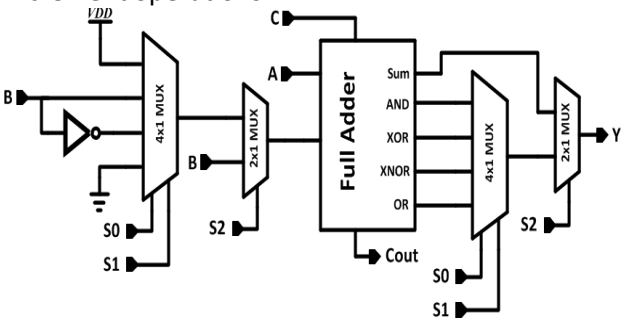


Fig.5.Schematicof1-BitALUStage

The 4-Bit ALU was built using four stages, as depicted in Fig. 6. S1 selects the logic 1 needed

for subtraction and increment operations, while the other values do not affect the results of the logical operations.

III.

SIMULATIONRESULTSANDCOMPARISON

At 65nm CMOS in Microwind, PMOS transistors are three times the size of NMOS transistors to maximize power consumption and delay performance in the proposed 4-bit ALU circuits. DSCH and microwind were used in the simulations, along with a 1V power source. As setinputs, we'll use A=1111, B=1010.DSCH 3.5 was used to simulate some of the operations using full swing GDI, and the results and digita

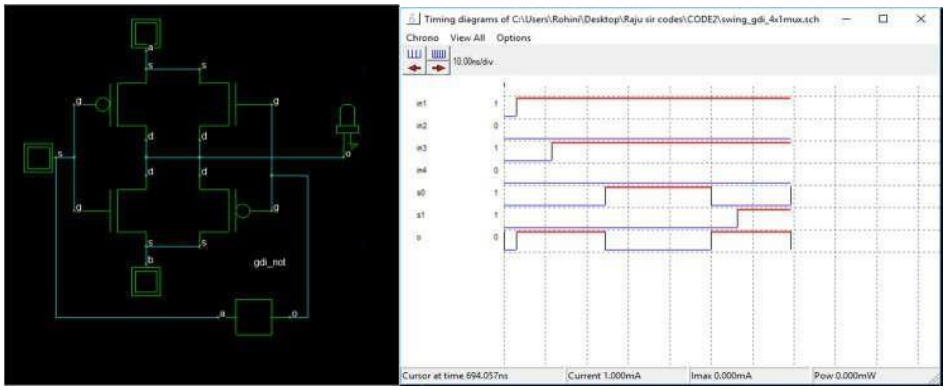


Fig.7Schematicof2x1muxdesignedusingDSCH3.5

Fig.8simulationoutputof2x1muxusingfullswingGDIinDSCH3.5

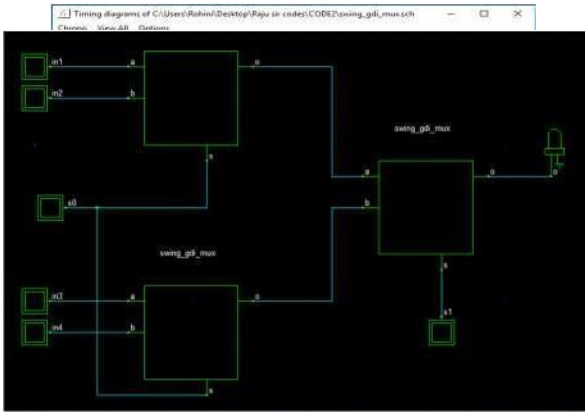


Fig.10simulationresultof4x1muxinDSCH3

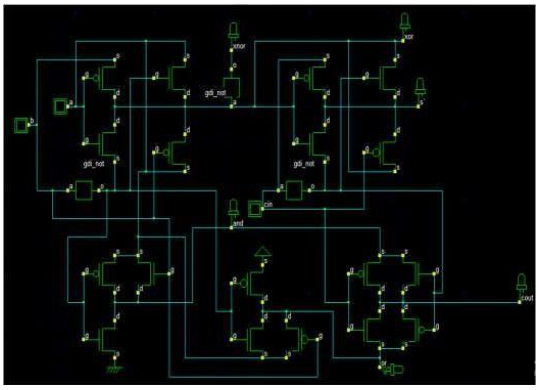


Fig. 11 schematic of proposed full swing GDIbased fulladder designedusingDSCH3.5

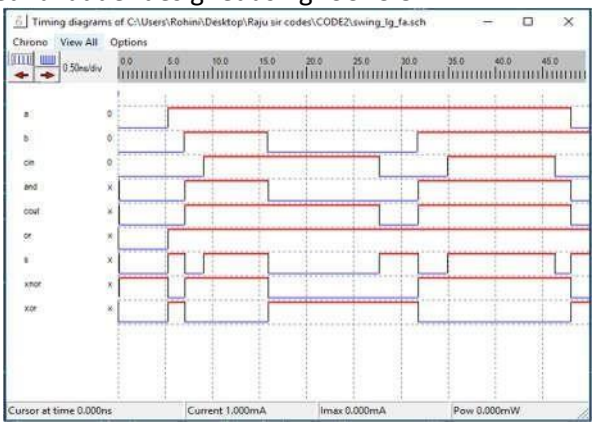


Fig. 12 simulation result of proposed full adderusingFSGDIinDSCH3.5.

Fig.14simulationresultofproposedALUusing

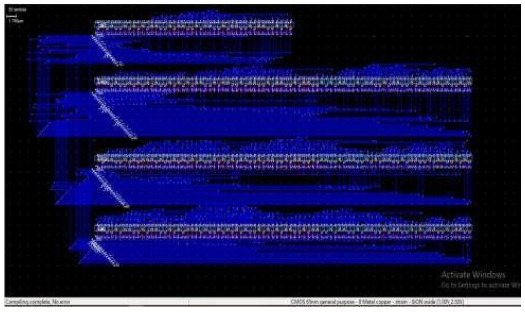
DSH3.5tool.

Fig. 16 shows the waveform of the proposedALU,Theresultsoftheproposeddesigncompared with the 4-Bit ALU existing design areshown inTableIII.

Fig. 16 The MICROWING 3.5 tool was used to simulate the proposed ALU in full swing. When it comes to power consumption and transistor count, the proposed ALU design beats out the competition hands down. The proposed ALU's power consumption is at or below the minimum values required by the specification. The number of transistors is also reduced when compared to other systems.

TABLEIII.COMPARISION

DESIGN	No"of transistors	Power(μW)
ALUwithCMOS gate	592	1.756
ALUwithGDI basedfulladder	416	1.253
Proposed ALUwith full swingGDIbasedfull adder.	296	0.095



IV. CONCLUSION

For the purpose of this study, we show a 4-Bit ALU implemented in 65nm CMOS utilizing the Full-Swing GDI approach and modelled in DSCH/MICROWIND. When it comes to power consumption and transistor count, the proposed ALU design has an advantage over the current design. The transistor-based architecture is powered by a 1V supply source.

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Fig.15layoutofproposedALUusingfullswingGDIimplementedon65 nmCMOStechnologyusing MICROWIND3.5tool.

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